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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,817	02/03/2004	Takaaki Negoro	R2180.0189/P189	9540

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EXAMINER	
SOWARD, IDA M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,817	NEGORO ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *22 and 23* is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,13,14,20 and 21* is/are allowed.

6)☒ Claim(s) *1,8 and 15* is/are rejected.

7)☒ Claim(s) *1-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2-3-04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-3-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed May 3, 2005.

Election/Restrictions

Applicant's election with traverse of claims 1-22 in the reply filed on May 3, 2005 is acknowledged. The traversal is on the ground(s) that "If the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to distinct or independent inventions." This is not found persuasive because searching the method (implanting, patterning, masking, thermal processing,...) of forming a semiconductor device requires a different thought process and class in searching than the semiconductor device structure.

The requirement is still deemed proper and is therefore made FINAL.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

Claims 1, 6-8, 13-15 and 20-21 are objected to because of the following informalities: "**of**" should have been **in** in

page 56, line 8;

page 58, line 11;

page 59, line 19;

page 60, line 18;

page 62, line 21;

page 64, line 3;

page 65, line 4;

page 67, line 12; and

page 68, line 21, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazato et al. (5,386,135).

In regard to claim 1, Nakazato et al. teach a semiconductor device, comprising: a P-type semiconductor substrate P-Sub; a P-channel DMOS transistor pMOS3 disposed on the P-type semiconductor substrate P-Sub and including a drain P formed of the P-type semiconductor substrate P-Sub and a source P formed in the P-type

semiconductor substrate P-Sub on a main surface of the P-type semiconductor substrate P-Sub; and a CMOS transistor disposed on the P-type semiconductor substrate P-Sub and including a P-channel MOS transistor pMOS2 formed in an N-type region nW2 formed in the P-type semiconductor substrate P-Sub on the main surface of the P-type semiconductor substrate P-Sub and an N-channel MOS transistor n mOS2 formed in a P-type region PW2 formed in the P-type semiconductor substrate P-Sub on the main surface of the P-type semiconductor substrate P-Sub, the P-type region PW2 being electrically isolated from the P-type semiconductor substrate P-Sub by the N-type region nW2 (Figure 33, column 33, lines 7-41).

In regard to claim 8, Nakazato et al. teaches that it is inherent in the art of semiconductor device interchange the conductivity type of the various region of the device (Figures 43-44, column 37, lines 3-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato et al. (5,386,135).

Nakazato et al. teach a semiconductor device comprising: a P-type semiconductor substrate P-Sub; a transistor including a P-channel DMOS transistor

pMOS3 disposed on the P-type semiconductor substrate P-Sub and including a drain P formed of the P-type semiconductor substrate P-Sub and a source P formed in the P-type semiconductor substrate P-Sub on a main surface of the P-type semiconductor substrate P-Sub; and a CMOS transistor disposed on the P-type semiconductor substrate P-Sub and including a P-channel MOS pMOS2 transistor formed in an N-type region nW2 formed in the P-type semiconductor substrate P-Sub on the main surface of the P-type semiconductor substrate P-Sub and an N-channel MOS transistor nMOS2 formed in a P-type region pW2 formed in the P-type semiconductor substrate P-Sub on the main surface of the P-type semiconductor substrate P-Sub, the P-type region pW2 being electrically isolated from the P-type semiconductor substrate P-Sub by the N-type region nW2.

In regard to a fixed voltage circuit, an output transistor and a controller, "If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) ("where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation"); Kropa v. Robie, 187 F.2d at 152, 88 USPQ2d at 480-81".

However, Nakazato et al. fail to teach the controller is configured to compare an output voltage from the output transistor with a reference voltage and provide feedback such that the output voltage remains constant.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure, as taught by Nakazato et al., so that the controller is configured to compare an output voltage from the output transistor with a reference voltage and provide feedback such that the output voltage remains constant to obtain the desired electrical performance from the semiconductor structure.

Allowable Subject Matter

Claims 6-7, 13-14 and 20-21 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as but not limited to a P-type semiconductor substrate including a P-type high concentration semiconductor substrate, a first P-type low concentration epitaxial layer, and a second P-type low concentration epitaxial layer, the P-type high concentration semiconductor substrate being disposed opposite to the main surface of the P-type semiconductor substrate, the second P-type low concentration epitaxial layer being disposed over the P-type high concentration semiconductor substrate, and the

first P-type low concentration epitaxial layer being disposed over the second P-type low concentration epitaxial layer; wherein the N-type region comprises a bottom portion including an N-type buried layer which is disposed at an interface of the first P-type low concentration epitaxial layer and the second P-type low concentration epitaxial layer.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Claims 2-5, 9-12 and 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor devices having DMOS and CMOS structures:

Boden, Jr. et al. (US 6,380,004 B2)

Contiero et al. (5,589,405)

Contiero et al. (5,610,421)

Erdeljac et al. (5,408,125)

Garnett et al. (5,556,796)

Harada et al. (6,844,578 B2)

Lee et al. (6,025,621)

Negoro et al. (US 6,911,694 B2)

Pearce (5,777,362)

Williams et al. (5,541,125)

Yamamoto et al. (US 6,359,318 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
July 6, 2005